# PSEUDOMORPHIC POWER HEMT WITH 53.5% POWER-ADDED EFFICIENCY FOR 1.9-GHz PHS STANDARDS

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## Abstract

We demonstrate a power-added efficiency of 53.5% at a very low idling current of 13 mA with a drain bias of 3 V in a proposed power amplifier. This amplifier meets the standards for the 1.9-GHz Japanese Personal Handy-phone System (PHS) which requires highly linear amplifiers, and this is the highest power-added efficiency and the lowest idling current so far reported. The proposed power amplifier uses a pseudomorphic high electron mobility transistor (PHEMT) which provides high transconductance, high linearity, and low idling current operation. This PHEMT was fabricated by using advanced power-device technology: the GaAs/InGaAs/GaAs PHEMT structure has a 0.35-μm gate made using phase-shifting lithography and a high In mole ratio (0.35) InGaAs channel.

## Introduction

Portable mobile communication systems require low-power-consumption components that operate at low supply voltages to extend battery life. This is especially true for the power amplifier used in the transmitter because it accounts for 30%-50% of the total power consumption. Moreover, digital portable phone systems that include a QPSK (quadrature phase shift keying) modulator, especially the 1.9-GHz Japanese Personal Handy-phone System (PHS), require a low-distortion power amplifier.

To lower power consumption, a highly efficient power amplifier that operates at a low idling current is required. But, for a system that requires low-distortion, low idling current operation is difficult to achieve with high efficiency because the low idling current generally increases distortion. Reports to date have shown 45% power-added efficiency at a low idling current of 40 mA with a drain bias of 3 V at 1.9 GHz[1], and 26.4% power-added efficiency at an idling current of 83 mA with a drain bias of 2.7 V at 1.9 GHz[2], when evaluated under the standards for the 1.9-GHz PHS. However, there have been no reports of highly efficient linear power devices with power-added efficiency over 50% that can operate at an idling current below 20 mA while meeting the standards for the 1.9-GHz PHS[1-4].

In this paper, a technique is proposed to increase the power-added efficiency with sufficient linearity under a very low idling current. This technique requires the use of transistors with high transconductance gm (i.e., those that have a thin channel layer, a short gate length, and a high indium mole ratio InGaAs channel layer).

## Power-added Efficiency Improvement by Optimization of the Load Impedance

This technique is shown in Fig. 1. An inclined load line, that is, a low drain conductance load, leads to a decrease in the knee voltage (Vk2→Vk1) and consequently an increase in the efficiency. However, under this condition, the drain current Ids is reduced (Ids2→Ids1) and the output power is decreased. The idling current is also reduced and distortion is increased.

To overcome these drawbacks, we use transistors with high gm under a low idling current. When these transistors are used under a low idling current, the self-biasing level, that is the idling current, can be raised during high signal operation and distortion is reduced. Also, the dynamic voltage swing can be increased and the output power increased.

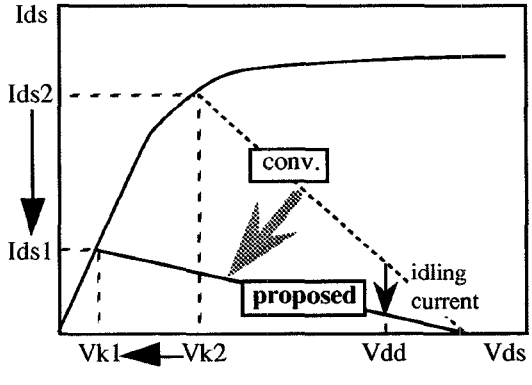


Fig. 1. Power-added efficiency improvement by optimization of the load impedance



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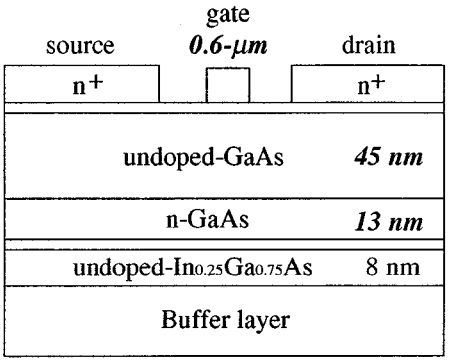
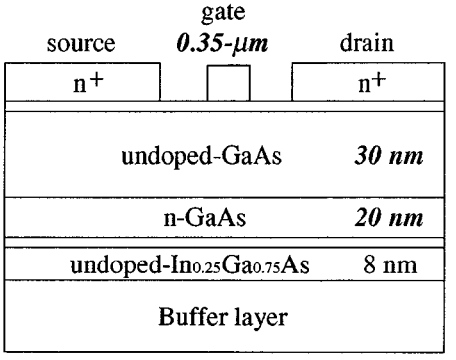
## Device Description

A cross-sectional view of the proposed pseudomorphic high electron mobility transistor (PHEMT), which was fabricated on an MBE-grown wafer, is shown in Fig. 2. The GaAs/InGaAs PHEMT has lower source resistance and higher linearity than an AlGaAs/InGaAs PHEMT[5] because high signal operation is limited by the low mobility of the AlGaAs channel layer. As shown in Fig. 2, to attain high gm, the proposed PHEMT has a thinner channel layer and a shorter gate length (0.35 μm), made with phase-shifting lithography, than the conventional structure[6]. Also, the gm can be further increased by increasing the In mole ratio to 0.35 in the InGaAs channel PHEMT[7]. A cross-sectional view of the proposed PHEMT gate structure is shown in Fig. 3. By using phase-shifting lithography with an optical 1/5 stepper, we obtained a 0.35-μm gate without having to use expensive electron beam lithography.




(a) conventional structure

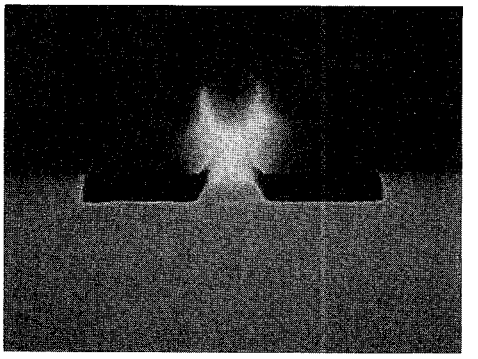



(b) proposed PHEMT structure

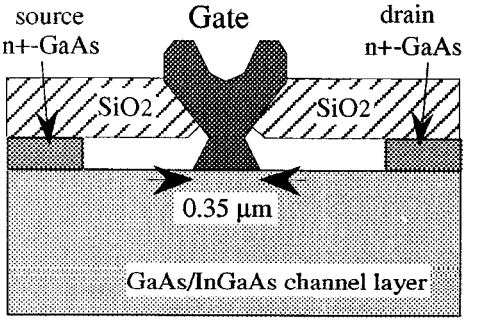
Fig. 2. Cross-section of the proposed PHEMT power device

## Results and Discussion

The power characteristics of the proposed PHEMT structure and the conventional structure evaluated under the standards for the 1.9-GHz Japanese Personal Handy-phone System (PHS) are compared in Fig. 4. Both of these power devices have a total gate width of 3.6 mm and a unit finger width of 200 μm. Their adjacent channel leakage power is -60 dBc at 1.9 GHz +/- 600 kHz when tested at the rated output power. The proposed structure exhibits a high power-added efficiency of 50.7% with an output power of 0.13 W at an very low idling current of 20 mA, and its output power is over 1.6 times higher than that of the conventional structure. Moreover, when a high In mole ratio InGaAs channel structure is used, it exhibits a very high power-added efficiency of 53.5%, compared to 42.5% with the conventional structure, and an output power of 0.11 W at an ultra-low idling current of 13 mA. Figure 5 shows the output-power spectrum of the proposed power amplifier for a π/4-shift QPSK-modulated source. These results demonstrate that the proposed PHEMT power device is very suitable for highly linear digital handy-phone systems.



(a) SEM photograph




(b) schematic view of (a)

Fig. 3. Cross-sectional view of the proposed PHEMT gate structure

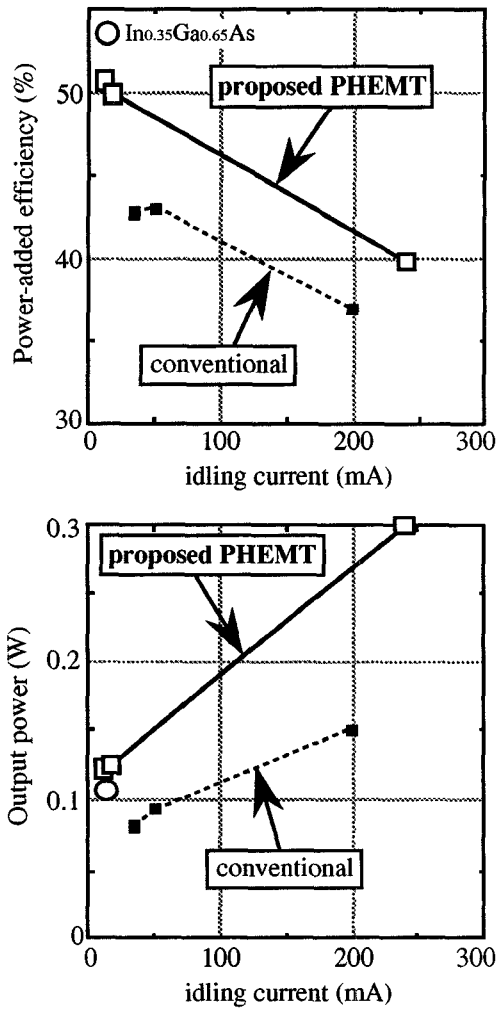



Fig. 4. Power performance as a function of idling current under the 1.9-GHz PHS standards with a drain bias of 3V

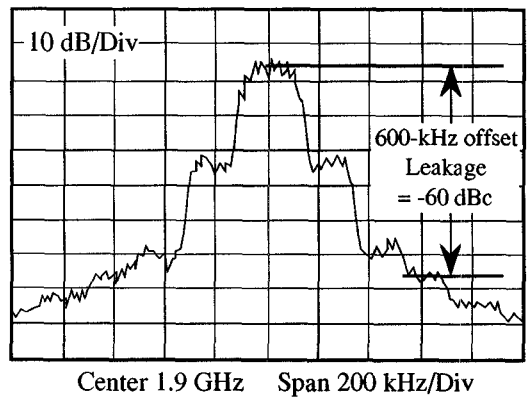



Fig. 5. Output spectrum for QPSK operation

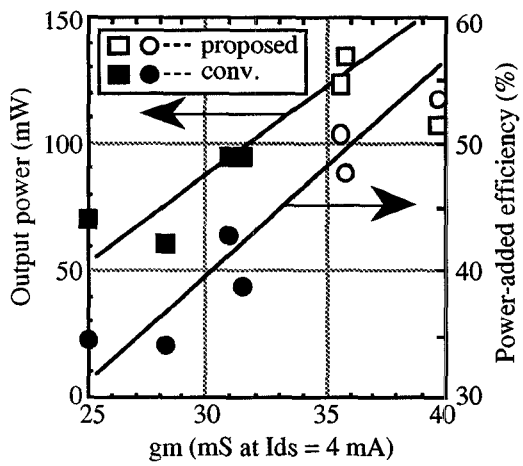



Fig. 6. Power performance as a function of gm for the 1.9-GHz PHS standards with a drain bias of 3V

Table 1. Comparison of the output power and power-added efficiency of power devices at a low drain bias

| Reference | this work | Muraguchi's work [1] | Nagaoka's work [2] |
|---|---|---|---|
| Efficiency under 1.9-GHz PHS standards (%) | 53.5 | 45 | 26.4 |
| Power under 1.9-GHz PHS standards (W) | 0.11 | 0.16 | 0.07 |
| idling current (mA) | 13 | 40 | 83 |
| adjacent leakage power (600 kHz off)(-dBc) | 60 | 57 | 58 |
| Drain Bias (V) | 3 | 3 | 2.7 |
| Frequency (GHz) | 1.9 | 1.9 | 1.9 |
| device structure | FET | MMIC | FET |

Figure 6 shows the transconductance at Ids = 4 mA in a 400-μm-wide PHEMT device versus the output power and power-added efficiency of both proposed and conventional PHEMT power devices operating at a low idling current. The output power and power-added efficiency of the PHEMT power devices are strongly related to the transconductance, and higher transconductance results in higher output power and efficiency. These results indicate that higher output power and efficiency than we report here can be attained.

The output power and power-added efficiency of power devices operating at a low drain bias are compared in Table 1. The proposed PHEMT power device exhibits power-added efficiency that is 8.5% higher and an idling current that is less than half that of Muraguchi's work[1].

## Conclusions

We have demonstrated a highly efficient GaAs/InGaAs/GaAs PHEMT power amplifier that offers a linear power-added efficiency of 53.5% at an ultra-low idling current of 13 mA with a 3-V drain bias under the standards for the 1.9-GHz Japanese Personal Handy-phone System. These results show that the proposed PHEMT power amplifier is well suited for use in digital portable phone systems which require highly linear devices. Power amplifiers for Class B operation (where the idling current is close to 0 mA) are expected to be developed with advances in PHEMT technology.

## Acknowledgments

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